What we claim is:

1. An IC chip comprising at least one externally and selectively cuttable member having at least one cuttable section, the cuttable member including a multiplicity of cuttable points, wherein said cuttable member remain cut open so long as at least one cuttable point remains cut open.

2. The IC chip according to claim 1, wherein said cuttable section is made of polysilicon.

3. The IC chip according to claim 1, wherein said multiple cuttable points are formed in series.

4. The IC chip according to claim 3, wherein said cuttable member includes at least one cuttable section having a linear portion of a uniform width.

5. The IC chip according to claim 3, wherein said diccectible section has alternating wide portions and narrow portions connected in series.

6. The IC chip according to claim 3, wherein said cuttable member comprises a multiplicity of series of cuttable sections which has a narrow portion formed between two wide portions.

7. The IC chip according to claim 1, wherein said cuttable member includes a multiplicity of cuttable sections which are coupled at one ends thereof with the same electric potential and coupled at the other ends thereof

with respective logic circuits.

8. The IC chip according to claim 7, wherein said cuttable sections have a linear portion of a uniform width.

9. The IC chip according to claim 7, wherein each of said cuttable sections has a narrow portion formed between two wide portions.

10. A semiconductor device, comprising:

an IC chip having

at least one externally and selectively cut member including at least one cut section, the cut member including a multiplicity of cut points, said cut member working normally when at least one of said cut points remains cut open, and

bumps formed on the same side of the IC chip as the cut member in association with respective cut points;

a substrate/another IC chip; and

a connection member made of an anisotropic conductor and sandwiched between said IC chip and said substrate/another IC chip, wherein

said IC chip and said substrate/another IC chip are pressed together.

11. The semiconductor device according to claim 10, wherein said cut section is made of polysilicon.

12. The semiconductor device according to claim 10, wherein said multiple cut points are formed in series.

13. The semiconductor device according to claim 12, wherein said cut member includes at least one cut section having a linear portion of a uniform width.

14. The semiconductor device according to claim 12, wherein said cut section has alternating wide portions and narrow portions connected in series.

15. The semiconductor device according to claim 12, wherein said cut member comprises a multiplicity of series of cut sections which has a narrow portion formed between two wide portions.

16. The semiconductor device according to claim 10, wherein said cut member includes a multiplicity of cut sections which are coupled at one ends thereof with the same electric potential and coupled at the other ends thereof with respective logic circuits.

17. The semiconductor device according to claim 16, wherein said cut sections have a linear portion of a uniform width.

18. The semiconductor device according to claim 16, wherein each of said cut sections has a narrow portion between two wide portions.